IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 1, 3, 10, 11, and 13. These sheets, which include Figs. 1, 3, 6, 10, 11, and 13, replace the original sheets including Figs. 1, 3, 6, 10, 11, and 13.

Attachment: Replacement Sheets (4)

REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

I. Status of the Claims

Claims 1-34 were pending and at issue in this patent application. By this amendment, claims 3 and 12 have been cancelled. Therefore, claims 1, 2, 4-11, 13-34 are now pending and at issue.

II. Summary of Office Action dated August 17, 2010

The drawings have been objected to for not having a legend that lists each identified element in the figures. Claim 3 has been rejected under 35 U.S.C. §112, second paragraph. Claims 1-34 have been rejected under 35 U.S.C. §102(b) as anticipated Snyder (U.S. Patent No. 6,507,214).

III. Response

Statement of the Substance of the Interview of September 10, 2010

Initially, applicant's representative would like to thank Examiner Treat for the telephonic interview on Sept 10, 2010. During the interview, the parties discussed the drawings objection.

Objection to Drawings

The specification has been amended to include a listing of element identifiers. Figs. 1, 3, 10, 11, and 13 have been amended to include legends identifying certain terms of the claims. Accordingly, applicant requests the withdrawal of the objection to the drawings.

Rejection under 35 USC 112, 2nd paragraph: Claim 3

The examiner rejected claim 3 under 35 U.S.C. 112, 2nd paragraph. Claim 3 has been cancelled. Thus, applicant submits this ground for rejection is moot.

Rejection under 35 USC 102(b): Claims 1-29

Applicant respectfully requests reconsideration of the rejection of claims 1, 2, 4-11, and 13-29 under 35 U.S.C. 102(b) as anticipated by Snyder.

To aide in the examiner's understanding, applicant provides a copy of independent claim 1, along with, in parentheses, reference numbers identifying examples, which are included by the terms of the claimed subject matter and which examples are illustrated by Figs. 1 and 3. Independent claim 1 recites:

> 1. A control method for controlling a data processing system including a logic circuit region (10) where circuits are dynamically reconfigurable, the control method comprising:
>
> a step of obtaining an architecture code (20), the architecture code (20) including object circuit information (23) for mapping an object circuit (19) that is at least part of a circuit for executing an application onto part of the logic circuit region(10), interface circuit information (24) for mapping an interface circuit (18) in contact with the object circuit (19) onto the logic circuit region (10), and boundary condition (26) to be realized in the interface circuit (18);
>
> a step of mapping the object circuit (19) and the interface circuit (18) in contact with the object circuit (19) onto the logic circuit region (10) according to the object circuit information (23) and the interface circuit information (24) of the architecture code (20); and
>
> an activating step of controlling the interface circuit (18) based on the boundary condition (26) of the architecture code (20).

Independent claims 9, 26, and 28 include similar functionality. Therefore, arguments on behalf of independent claim 1 apply similarly to claims 9, 26, and 28.

Snyder is directed to digital configurable macro architecture designed to be configurable because of its programmable 8-bit circuit modules, which provide one of a variety of predetermined digital functions by changing the content of registers 50 of the 8-bit modules.

In particular, Snyder describes an already structured programmable digital circuit block 100, which includes programmable configuration registers 50. Snyder only describes programming its registers 50 via a bus 90. (Snyder, col. 3, lines 3-18.) Snyder does not provide any solution as to how to divide circuits onto a region. Snyder does not describe

mapping the object circuit and the interface circuit in contact with the object circuit onto the logic circuit region according to the object circuit information and the interface circuit information, as recited in claims 1, 9, 26, and 28.

Accordingly, Snyder does not describe or suggest every element of the independent claims 1, 9, 26, and 28. Dependent claims 2-8, 10-25, 27, and 29 depend respectively from independent claims 1, 9, 26, and 28 and should be allowed for at least the reasons stated above. Therefore, applicant respectfully requests withdrawal of the 35 U.S.C. 102(b) rejection of claims 1, 9, 26, and 28, and claims dependent therefrom.

Rejection under 35 USC 102(b): Claims 30-34

With respect to claims 30-34, of which claim 30 is the independent claim to which claims 31-34 depend, Snyder does not describe or suggest at least, "the [reconfigurable] elements [of the logic circuit, which] respectively include an operation core that performs a logic operation on input data and outputs output data, the operation core including a selector into which a multibit function code for designating the logic operation is inputted and which selects the output data according to the input data."

According to Snyder, the configuration register 50 configures the cascade inputs 60 and cascade outputs 70 of the programmable circuit block 100 to interface with another programmable digital circuit block 100. (Snyder, col. 5, line 66 to col. 4, line 12.)

The claimed reconfigurable element performs two functions, namely it performs a logic operation on input data and it outputs output data, wherein the designated logic operation selects the output data according to the input data.

In Snyder the configuration registers 50 are reconfigurable. However, the reconfigurable configuration registers 50 of Snyder do not comprise an operation core, much less "an ***operation core (e.g., 65) [of the reconfigurable elements (e.g., 53) of the logic circuit region (e.g., 10)]*** that ***performs a logic operation on input data and outputs output data***," much less "the operation core including a selector (e.g., 66) into which a multibit function code for designating the logic operation is inputted and which selects the output data ***according to the input data***." (See pars. 92-96 of the application specification.)

In particular, par. 92 of the application specification states an example where, "the divided circuits 19 are mapped so as to consume one or a plurality of circuit blocks 51." The

example circuit block 51 includes a plurality of elements (53) which respectively include an operation core 65. FIG. 13 illustrates an example configuration of the operation core (rxe_core) 65. The example operation core 65 includes a selector 66 that has a 16-bit function code φf for designating a logic operation as an input and selects the output data φo according to the input data φi. Snyder's configuration register 50 simply does not amount to the recited reconfigurable element," much less "an operation core [of the reconfigurable elements of the logic circuit region] that performs a logic operation on input data and outputs output data, the operation core including a selector into which a multibit function code for designating the logic operation is inputted and which selects the output data according to the input data."

Accordingly, Snyder does not describe or suggest every element of independent claim 30. Dependent claims 31-34 depend from independent claim 30 and should be allowed for at least the reasons stated above. Therefore, applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. 102(b) of independent claim 30, and claims 31-34, depending there from.

IV. Conclusion

For the foregoing reasons, applicant respectfully requests reconsideration and allowance of claims 1, 2, 4-11, and 13-34.

The Commissioner is hereby authorized to charge any additional fees that are required for the consideration of this paper and to credit any overpayments to Deposit Account No. 13-2855 of Marshall, Gerstein & Borun LLP. In addition, if an additional petition for an extension of time under 37 C.F.R. 1.136(a) is necessary to maintain the pendency of this case and is not otherwise requested in this case, applicant requests that the Commissioner consider this paper to be a request for an appropriate extension of time and hereby authorize the Commissioner to charge the fee as set forth in 37 C.F.R. 1.17(a) corresponding to the needed extension of time to Deposit Account No. 13-2855 of Marshall, Gerstein & Borun LLP.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicant respectfully requests that the Examiner call its attorney at the number listed below.

Dated: January 14, 2011

Respectfully submitted,

By _____

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